this will automatically be slowed down or speeded up, as the case may be, due to the alternating delay values. In this way, the circuit becomes an oscillator locked at frequency $f_{in}/2$, and thereby forms a frequency divider, since f_{in} is the frequency of the input signal IN/INB. When viewed in this way, the operation of the circuit can be likened to a so-called parametric amplifier.

Please amend the paragraph beginning on page 9, line 32, and ending on page 10, line12, as follows:

Figure 5 schematically shows the input/output characteristic of each amplifier 40a and 40b shown in Figure 4 including hysteresis. The overall negative feedback (due to the coupling from the Q output of the second stage to the DB input of the first) overcomes the positive feedback necessary to create hysteresis of each latch. The effect of this is such that by changing the hysteresis the effective propagation delays (T_1 and T_2) through the amplifiers change, while the strength of the connections between the amplifiers remains constant. In particular, if delays T_1 and T_2 are made to vary cyclically, with frequency f_{in} about a value of [$1/f_{in}$, (i.e. $1/f_{in} < T_1$ and $T_2 > 1/f_{in}$)] $\underline{1/[2f_{in}]}$, $\underline{\text{(i.e. } 1/[2f_{in}] < T_1 \text{ and } T_2 > 1/[2f_{in}]\text{)}}$ such that when T_1 increases T_2 decreases and vice versa then, as in the first embodiment, the logic high and lows can only propagate around a circuit with frequency [$1/2f_{in}$] $\underline{f_{in}/2}$.

IN THE CLAIMS

Please cancel claims 1-30 without prejudice.

Please add the following new claims 31-58.

31. (New) A frequency divider circuit comprising:

a first signal generator operable to generate a first periodic signal to be frequency divided by the frequency divider circuit;

a second signal generator operable to generate a second periodic signal which is in anti-phase with the first periodic signal; and

an even number of amplifier stages connected in series, with an output of a last amplifier stage connected to an input of a first amplifier stage and each amplifier stage having an associated

propagation delay which varies in response to a respective control signal; wherein the first signal generator is coupled to an or each odd amplifier stage in order to apply said first periodic signal as said control signal for the or each odd amplifier stage and the second signal generator is coupled to an or each even amplifier stage in order to apply said second periodic signal as said control signal for the or each even amplifier stage so that the propagation delay through the or each even amplifier stage decreases when the propagation delay through the or each odd amplifier stage increases; and

wherein said first and second signal generators are arranged to generate said first and second periodic signals such that the propagation delay through each of the amplifier stages is modulated about half the period of said first and second periodic signals.

32. (New) A frequency divider circuit according to claim 31, wherein there are two amplifier stages connected in series.

33. (New) A frequency divider circuit comprising a plurality of frequency divider circuits according to claim 31 connected in series.

34. (New) A frequency divider circuit according to claim 31, wherein each amplifier stage comprises a differential amplifier.

35. (New) A frequency divider circuit according to claim 31, wherein each amplifier stage comprises connection logic circuitry, and wherein for each amplifier stage the reactive control signal is operable to vary the propagation delay through the connection logic circuitry.

36. (New) A frequency divider circuit according to claim 35, wherein said connection logic circuitry comprises at least one transistor having an associated variable resistance, and wherein said control signal is operable to vary said variable resistance in order to vary the propagation delay through the connection logic circuitry.

37. (New) A frequency divider circuit according to claim 31, wherein each amplifier stage

comprises an amplifier with an associated hysteresis.

38. (New) A frequency divider circuit according to claim 37, wherein for each amplifier stage the respective control signal is operable to vary the hysteresis of said amplifier.

39. (New) A frequency divider circuit according to claim 31, wherein said frequency divider circuit is a FET type semiconductor circuit.

40. (New) A frequency divider circuit according to claim 39, wherein said frequency divider circuit is integrated monolithically with complementary FET logic.

41. (New) A frequency divider circuit according to claim 39, wherein said frequency divider circuit is a CMOS circuit integrated monolithically with CMOS logic circuitry.

42. (New) A frequency divider circuit according to claim 39, wherein an input to each amplifier stage is formed by the gate of a field effect transistor.

43. (New) A frequency divider circuit according to claim 31, wherein the first signal generator is operable to generate the first periodic signal at a frequency greater than 100 MHz.

44. (New) A frequency divider circuit according to claim 31, further comprising logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two.

45. (New) A frequency divider circuit according to claim 31, wherein each of said amplifier stages comprises a latch circuit having first and second inverters connected in a memory arrangement with an output of the first inverter connected to an input of the second inverter.

46. (New) An frequency divider circuit according to claim 45, in which each of the first and

second inverters comprises a p-channel transistor and a n-channel transistor, and each latch circuit further comprises two pairs of n-channel transistors which are operable to control the state of said memory arrangement.

47. (New) An frequency divider circuit according to claim 46, wherein the aspect ratio of the n-channel transistor of each inverter is less than the aspect ratio of each of the controlling n-channel transistors.

48. (New) A method of frequency division using an even number of amplifier stages connected in series, with an output of a last amplifier stage connected to an input of a first amplifier stage and each amplifier stage having an associated propagation delay which varies in response to a control signal, said method comprising:

applying a first periodic signal to be frequency divided by the frequency divider circuit as the control signal for an or each odd amplifier stage and applying a second periodic signal which is in anti-phase with the first periodic signal as the control signal for an or each even amplifier stage so that the propagation delay through the or each even amplifier stage decreases when the propagation delay through the or each odd amplifier stage increases,

wherein said first and second periodic signals are arranged to modulate the propagation delay through each amplifier stage about half the period of said first and second periodic signals.

49. (New) A method according to claim 48, wherein each amplifier stage comprises a differential amplifier.

50. (New) A method according to claim 48, wherein each amplifier stage comprises connection logic circuitry, and wherein for each amplifier stage applying the respective control signal varies the propagation delay through the connection logic circuitry.

51. (New) A method according to claim 50, wherein said connection logic circuitry comprises at least one transistor having an associated variable resistance, and wherein applying said control

signal varies said variable resistance in order to vary the propagation delay through the connection logic circuitry.

52. (New) A method according to claim 48, wherein each amplifier stage comprises an amplifier with hysteresis.

53. (New) A method according to claim 52, wherein for each amplifier stage applying the respective control signal varies the hysteresis of said amplifier.

54. (New) A method according to claim 48, wherein said amplifier stages comprise an FET type semiconductor integrated circuit.

55. (New) A method according to claim 54, wherein said amplifier stages comprise a CMOS integrated circuit.

56. (New) A method according to claim 48, comprising applying the first periodic signal with a frequency greater than 100 MHz.

57. (New) A method according to claim 48, wherein said method comprises providing logic circuitry connected in series between at least two of the amplifier stages to enable division by ratios other than simple powers of two.

58. (New) A radio receiver comprising a frequency divider circuit comprising:

a first signal generator operable to generate a first periodic signal to be frequency divided by the frequency divider circuit;

a second signal generator operable to generate a second periodic signal which is in anti-phase with the first periodic signal; and

an even number of amplifier stages connected in series, with an output of a last amplifier stage connected to an input of a first amplifier stage and each amplifier stage having an associated